

In the claims:

1 1. (Original) A method of designing an integrated circuit, comprising:
2 identifying a programmable logic core;
3 identifying an application;
4 designing an application specific circuit for the application; and
5 integrating the programmable logic core into the designed application specific
6 circuit.

1 2. (Currently Amended) A method of designing an integrated circuit, comprising:
2 identifying a programmable logic core for the integrated circuit;
3 establishing a set of timing constraints associated with the programmable logic
4 core; and
5 controlling the design of application specific circuitry that interfaces with the
6 programmable logic core in the integrated circuit in accordance with the set of timing
7 constraints.

1 3. (Currently Amended) A method of designing an integrated circuit, comprising:
2 identifying a programmable logic core for the integrated circuit;
3 establishing a sign-off design associated with the programmable logic core; and
4 controlling the design of application specific circuitry that interfaces with the
5 programmable logic core in the integrated circuit in accordance with the sign-off design.

1 4. (Original) An integrated circuit, comprising:
2 a programmable logic core; and
3 application specific circuitry, the application specific circuitry being designed in
4 accordance with a sign-off design.

1 5. (Currently amended) An integrated circuit according to claim 4, wherein the
2 programmable logic core includes:
3 a programmable multi-scale array;

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4 an application circuit interface for providing a signal interface between the
5 programmable multi-scale array and the application specific circuitry; and
6 a programmable logic core adapter that configures the programmable multi-scale
7 array.

1 6. (New) The integrated circuit of claim 5, wherein the programmable multi-scale array
2 comprises an array of configurable arithmetic logic units supporting at least:
3 register transfer level functions; and
4 random logic structures.

1 7. (New) The integrated circuit according to claim 4, wherein the programmable logic
2 core comprises a programmable multi-scale array supporting functions of different scales.

1 8. (New) The integrated circuit according to claim 4, wherein the programmable logic
2 core includes ~~at~~ a programmable logic core control for loading configuration data into the
3 programmable logic core.

1 9. (New) The integrated circuit according to claim 4, wherein the programmable logic
2 core comprises:
3 an array of configurable logic structures having internal storage registers; and
4 a scratchpad memory to supplement the storage registers.

1 10. (New) The integrated circuit according to claim 4, wherein the programmable logic
2 core includes ~~at~~ a configuration test interface for data and control flow between the application
3 specific circuit and the programmable logic core.

1 11. (New) The integrated circuit according to claim 4 further comprising a
2 microprocessor core communicatively connected to the programmable logic core.

1 12. (New) The integrated circuit according to claim 4, wherein the programmable logic
2 core comprises blocks supporting:
3 configuration data control logic;

4 scan path logic; and
5 application circuit interface logic.

1 13. (New) The integrated circuit according to claim 4, wherein the programmable logic
2 core comprises arithmetic logic units including:
3 function cells; and
4 an arithmetic logic unit controller.

1 14. (New) The integrated circuit according to claim 4, wherein the programmable logic
2 comprises:
3 an internet protocol core; and
4 arithmetic logic units communicatively connected to the internet protocol core.

1 15. (New) The integrated circuit according to claim 4, wherein the programmable logic
2 core supporting:
3 an idle state that is entered after an assertion of a signal that power is good;
4 a built in self test state for testing the programmable logic core, the built in self test state
5 is entered from the idle state upon receipt of a test command;
6 a configuration state for implementing a configuration process, the configuration state
7 supports entry from the idle state and from the built in self test state after receipt of
8 a configuration clock signal; and
9 an operate state that controls operations of arithmetic logic units, and is entered after
10 completion of the configuration process.

1 16. (New) An integrated circuit, comprising;
2 means for performing functions associated with a programmable logic core; and
3 means for performing functions associated with application specific circuitry that is
4 designed in accordance with a sign-off design.

1 17. (New) An integrated circuit, comprising:
2 (I) application specific circuitry, the application specific circuitry being designed
3 in accordance with a sign-off design; and

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4 (II) a programmable logic core including at least
5 (A) a programmable multi-scale array having an array of configurable
6 arithmetic logic units supporting register transfer level functions,
7 random logic structures, and state machine structures,
8 (B) an application circuit interface for providing a signal interface
9 between the programmable multi-scale array and the application
10 specific circuitry, the application circuit interface having test registers
11 for testing the programmable logic core,
12 (C) scratchpad memories for supplementing storage of the
13 programmable multi-scale array,
14 (D) a configuration test interface for data and control flow between the
15 application specific circuit and the programmable multi-scale array,
16 (E) a programmable logic control for loading configuration data into the
17 multi-scale array, and
18 (F) a programmable logic core adapter that configures the programmable
19 multi-scale array through the configuration test interface.

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1 18. (New) A portion of programmable logic program flow comprising:
2 synthesizing data associated with a multi-scalable array and a program logic core design;
3 performing a programmable logic core mapping;
4 performing a programmable logic core placement;
5 performing a programmable logic core routing; and
6 performing a timing and netlist verification.
